CFP2-LR4 Transceiver
100G-BASE 10km CFP2

Features:

- Hot pluggable CFP2 MSA package
- 3.3V Power supply and MDIO management interface for digital diagnostics
- Duplex LC Connector Interface
- Integrated 4-LAN WDM TOSA/ROSA for up to 10km link over G.652 SMF
- Operating data rate at 103.125Gbps
- Compliant with 100GBASE-LR4
- CFP-MSA-CFP2-HW-Specification compliant
- Operating Case Temperature: 0 ~+70℃
- Power consumption less than 9W

Applications:

- 100GBase-LR4 Ethernet

Product Description

TC2-HG10-31DCR CFP2 transceivers are designed for use in 100 Gigabit Ethernet links over 10km single module fiber, and it compliant to the CFP2 MSA CFP2 HW and IEEE 802.3ba 100GBASE-LR4. Digital diagnostics are available via MDIO as specified in the CFP2 MSA Management Interface Specification. The transceiver's designs are optimized for high performance and cost efficiency to provide customers the best solutions for Datacom and Telecom applications. The transceiver is RoHS-6 compliant and lead-free per Directive 2002/95/EC.

Ordering information

Part No.	Data Rate	Laser	Fiber Type	Distance*Note1	Optical Interface	Bail color	Temp.*Note2	DDMI
TC2-HG10-31DCR	103.125G	4-LANE: 1295.56, 1300.05, 1304.58, 1309.14,	SMF	10km	LC	Blue	ST	YES

Note1: 10km with 9/125μm SMF

Note2: ST: 0 ~ +70deg C

Regulatory Compliance

Feature	Standard	Performance
Electrostatic Discharge (ESD) to the Electrical Pins	MIL-STD-883G Method 3015.7	Class 1C (>1000 V)
Electrostatic Discharge to the enclosure	EN 55024:1998+A1+A2 IEC-61000-4-2 GR-1089-CORE	Compliant with standards
Electromagnetic Interference (EMI)	FCC Part 15 Class B EN55022:2006 CISPR 22B :2006 VCCI Class B	Compliant with standards Noise frequency range: 30 MHz to 6 GHz. Good system EMI design practice required to achieve Class B margins. System margins depend on customer host board and chassis design.
Immunity	EN 55024:1998+A1+A2 IEC 61000-4-3	Compliant with standards. 1kHz sine-wave, 80% AM, from 80 MHz to 1 GHz. No effect on transmitter/receiver performance is detectable between these limits.
Laser Eye Safety	FDA 21CFR 1040.10 and 1040.11 EN (IEC) 60825-1:2007 EN (IEC) 60825-2:2004+A1 EN (IEC) 60950-1:2006+A1+A11+A12	CDRH compliant and Class I laser product. TUV Certificate No. R50271605
Component Recognition	UL and CUL EN60950-1:2006	TUV Certificate No. E344594 (CB:JPTUV-053877)
RoHS2.0	20011/65/EU	Compliant with standards

Absolute Maximum Ratings*Note3

Parameter	Symbol	Min	Max	Unit
Storage Temperature	TS	-40	+85	℃
Supply Voltage	V_{CC}	-0.3	3.6	V
Operating Humidity	-	5	85	%

Note3: Exceeding any one of these values may destroy the device permanently.

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Operating Case Temperature	Tc	0		70	°C
Power Supply Voltage	V_{CC}	3.14	3.3	3.47	V
Bit Rate			103.125		Gbps
Supply Current	Icc			3560	mA
Power dissipation	P			9	W
Low Power dissipation	P_{Low}			2	W
In-rush Current				200	mA/us
Turn-off rush Current		-200			mA/us

Performance Specifications – Electrical

Parameter	Symbol	Min	Typ.	Max	Unit	Notes
3.3V LVCOMS						
Input High Voltage	V_{IH}	2		Vcc+0.3	V	MOD_RSTn, MOD_LOPWR, TX_DIS, PRG_CNTL, MOD_ABS, RX_LOS, GLB_ALRMn, PRG_ALRM) are LVCMOS I/O
Input Low Voltage	V_{IH}	-0.3		0.8	V	
Input Leakage Current	I_{IN}	-10		10	mA	
Output High Voltage (IOH =-100uA)	V_{OH}	Vcc-0.2		Vcc+0.3	V	
Output Low Voltage (IOL =100uA)	V_{OL}	-0.3		0.2	V	
Minimum Pulse Width of Control Pin Signal	t_CNTL	100			us	
1.2V CMOS						
Input High Voltage	V_{IH}	0.84		1.5	V	MDIO, MDC, PRTADR(4:0) are 1.2V LVCMOS I/O
Input Low Voltage	V_{IL}	-0.3		0.36	V	
Input Leakage Current	I_{IN}	-100		100	uA	
Output High Voltage	V_{OH}	1	-	1.5	V	
Output Low Voltage	V_{OL}	-0.3		0.2	V	
Output High Current	I_{OH}			-4	mA	
Output Low Current	I_{OL}	4			mA	
Input capacitance	C_i			10	pF	
Reference Clock						
Impedance	Zd	80	100	120	ohm	
Frequency	1/64 of host lane rate					
Frequency Stability	Xf	-100		100	ppm	
Input Differential Voltage	Vdiff	400		1200	mV	
RMS Jitter	σ			10	ps	
Clock Duty Cycle		40		60	%	
Clock Rise/Fall Time 10/90%	Tr/f	200		1250	ps	

Timing Specifications

Parameter	Symbol	Min	Typ.	Max	Unit
Hardware MOD_LOPWR Assert	t_MOD_LOPWR_assert			1	ms
Hardware MOD_LOPWR De-assert	t_MOD_LOPWR_deassert			10	s
Receiver Loss of Signal Assert Time	t_loss_assert			100	us
Receiver Loss of Signal De-Assert Time	t_loss_deassert			100	us
Global Alarm Assert Delay Time	GLB_ALRMn_assert			150	ms
Global Alarm De-Assert Delay Time	GLB_ALRMn_deassert			150	ms
Host MDIO t_setup	t_setup	10			
Host MDIO t_hold	t_hold	10			
CFP2 MDIO t_delay	t_delay	0		175	
Initialization time from Reset	t_initialize			2.5	s
Transmitter Disabled (TX_DIS asserted)	t_deassert			100	us
Transmitter Enabled (TX_DIS de-asserted)	t_assert			2	ms
Management Interface Clock Frequency	F_MDC	0.1		4	MHz
Management Interface Clock Period	t_prd	250		10000	ns
MDC high and low time	twidth	40		60	%
		160			ns
MDIO/MDC termination in CFP2	Zt	100			kOhm

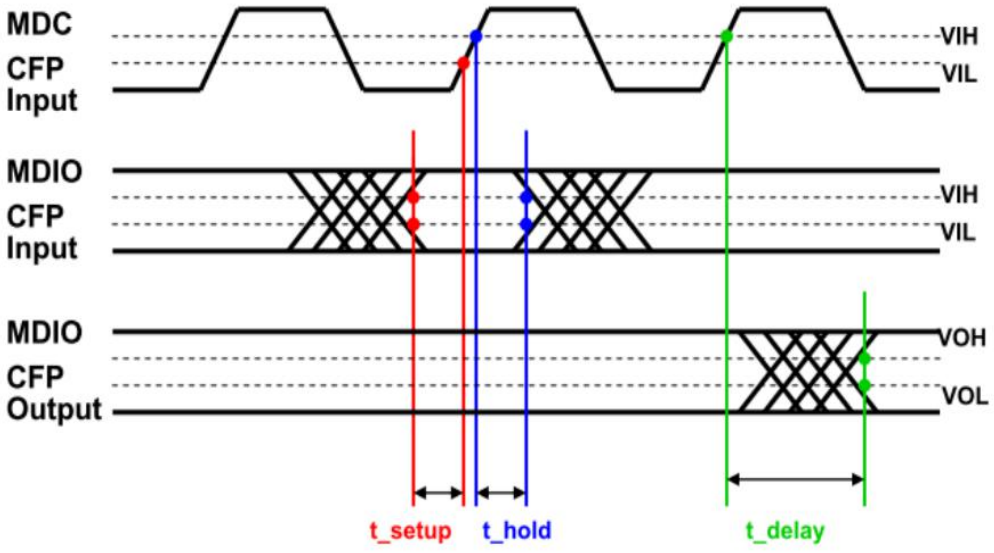

Figure 1. 100 Gb/s CFP2 MDIO & MDC Timing Diagram

Performance Specifications – Optical

(4-LANE WDM DFP and PIN， 10Km)

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Transmitter						
Channel data rate			25.7812		Gbps	
Data rate variation		-100		100	ppm	
Centre Wavelength	λc_{T0}	1294.53	1295.56	1296.59	nm	
	λc_{T1}	1299.02	1300.05	1301.09	nm	
	λc_{T2}	1303.54	1304.58	1305.63	nm	
	λc_{T3}	1308.09	1309.14	1310.19	nm	
Total Average Launch Power	Pout			10.5	dBm	
Average Launch Power per Lane	Pavg	-4.3		4.5	dBm	
Optical Modulation Amplitude per Lane	OMA	-1.3		4.5	dBm	
Difference in Launch power between any two lances(OMA)				5	dBm	
Launch power in OMA minus TDP, per lane	Pomatdp	-2.3			dB	
Extinction Ratio	ER	4	5.5		dB	
Average Launch Power of TX_DIS Transmitter per lane	P_{OFF}			-30	dBm	TX_dis=H
SMSR	SMSR	30			dB	
Dispersion Penalty	DP			2.2	dB	10km SMF
Relative Intensity Noise	RIN			-130	dB/Hz	Mod off
Optical Return Loss Tolerance	T_{RL}			20	dB	
Transmitter reflectance	Tef			-12	dB	
Optical Eye Mask {X1, X2, X3, Y1, Y2, Y3}			{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}			NOTE4
Receiver						
Channel data rate			25.7812		Gbps	
Data rate variation		-100		100	ppm	
Centre Wavelength	λc_{T0}	1294.53	1295.56	1296.59	nm	
	λc_{T1}	1299.02	1300.05	1301.09	nm	
	λc_{T2}	1303.54	1304.58	1305.63	nm	
	λc_{T3}	1308.09	1309.14	1310.19	nm	
Damage threshold	λc		5.5		dBm	
Average receiver power per Lane	Pin	-10.6		4.5	dBm	
Receive power OMA per Lane	Poma-in			4.5	dBm	
Receiver Sensitivity(OMA) per Lane	Psen			-8.6	dBm	
Stressed Receiver Sensitivity per Lane	Psen_str			-6.8	dBm	
Receiver Reflectance	Ref			-26	dB	

Vertical eye closure penalty per Lane		1.8	dB
Stressed eye jitter per Lane		0.3	UI
Rx-Lane LOS Assert	-18		dBm
Rx-Lane LOS De-assert		-12	dBm
Rx-Lane LOS Hysteresis	0.5		dB

Performance Specifications – Electrical

Parameter	Symbol	Min	Typ.	Max	Unit	Notes
Transmitter						
Signal Rate Per Lane			25.7812		Gbps	
Signal Rate Tolerance		-100		100	ppm	
AC Common-mode Input Voltage Tolerance(RMS)				20	mV	
Differential Input Return Loss		See Equation(83B-7) of IEEE802.3ba-2010			dB	
Total Input Jitter Tolerance	T_{jin}			0.62	UI	
Deterministic Input Jitter Tolerance	D_{jin}			0.42	UI	
Optical Eye Mask {X1, X2, X3, Y1, Y2, Y3}		{0.25, 0.4, 0.45, 0.25, 0.28,0.4}				Note4
Receiver						
Signal Rate Per Lane			25.7812		Gbps	
Signal Rate Tolerance		-100		100	ppm	
Single-ended Output Voltage		-0.4		4	V	
Output AC common-mode Voltage(RMS)				15	mV	
Output Transition Time	T_r	15			ps	20%~80%
Differential Output Return Loss		See Equation(83B-5) of IEEE802.3ba-2010			dB	
Total Jitter	T_j			0.43	UI	

Note4: Refer to figure 1

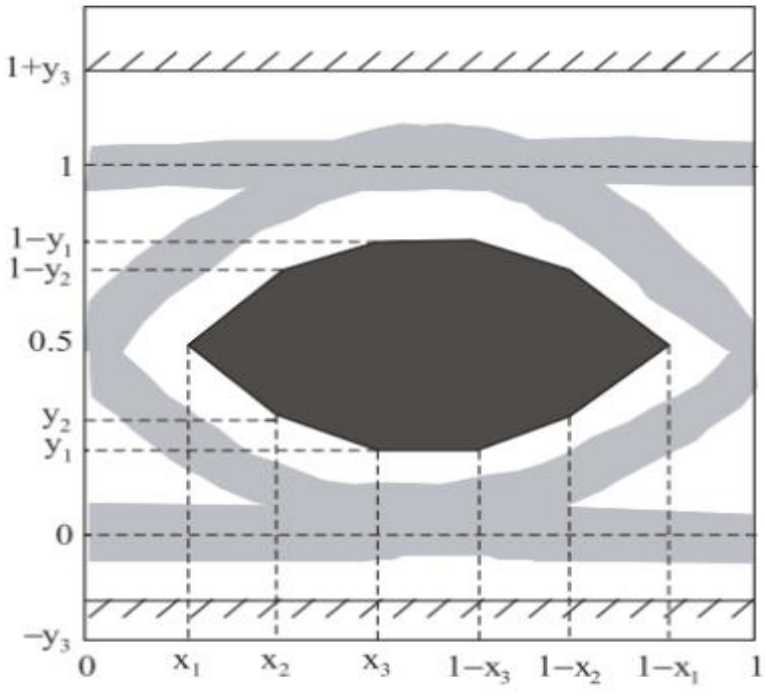

Figure 1. Transmitter eye mask definiton

Internal reference structure

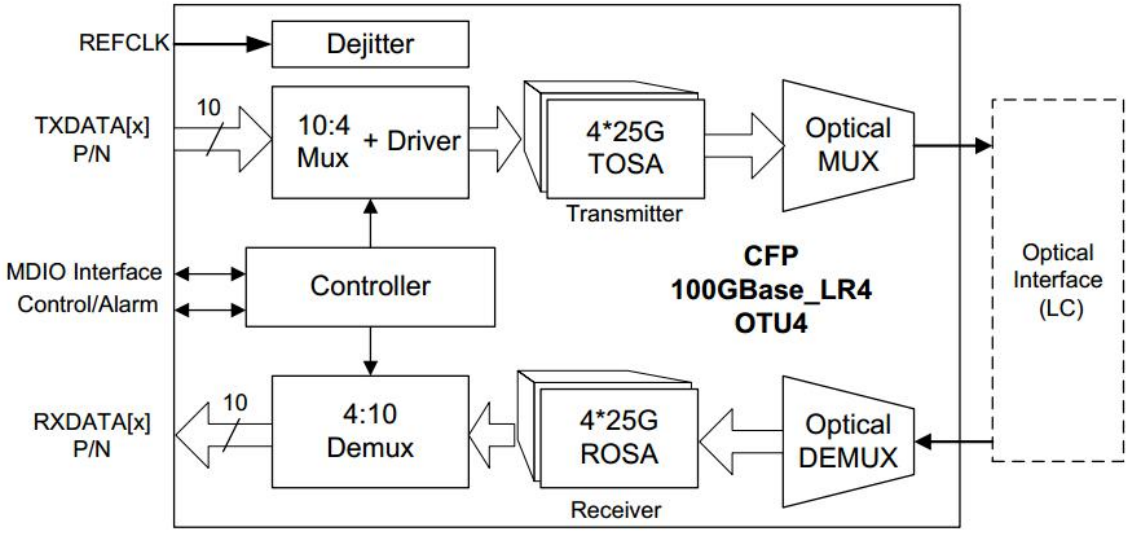

Figure 2. 10km 100Gb/s CFP2 internal structure

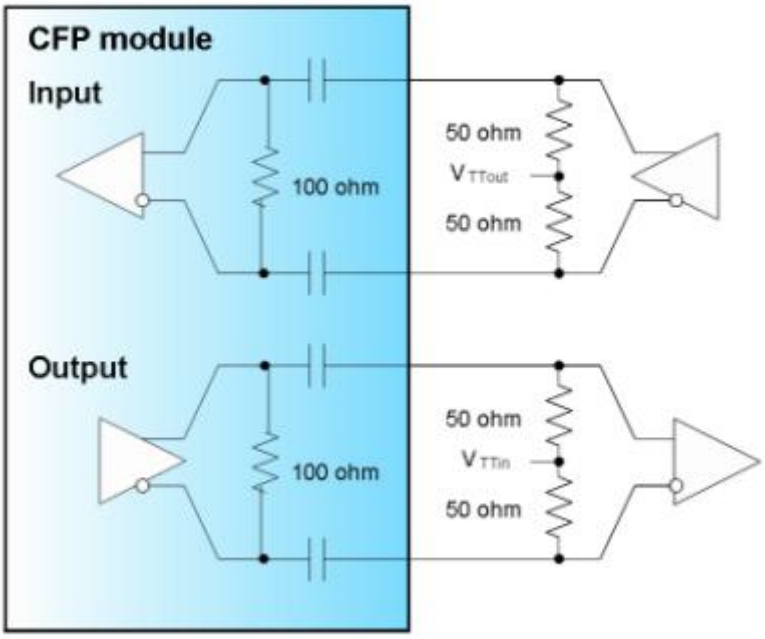

Figure 3. Recommended High Speed I/O for Data and Clocks

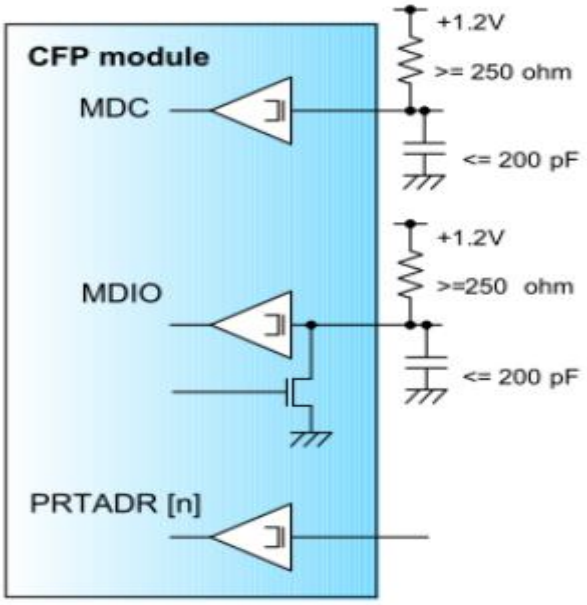

Figure 4. Recommended MDIO Interface Termination

Pin Layout

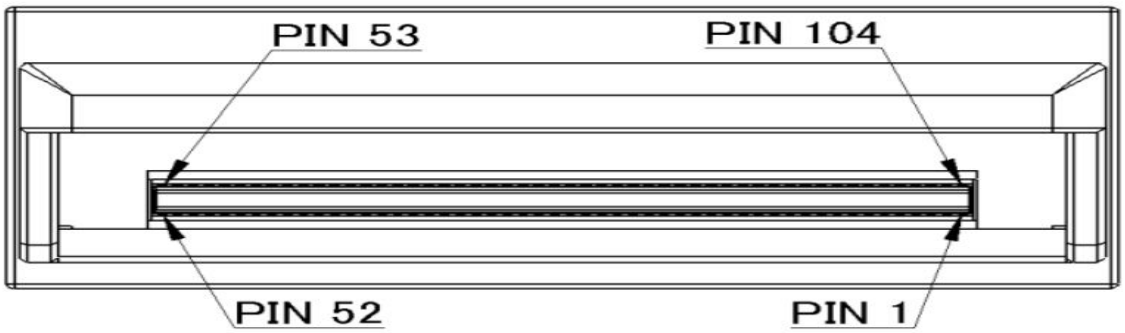

Figure 5. CFP2 Module Pad Layout

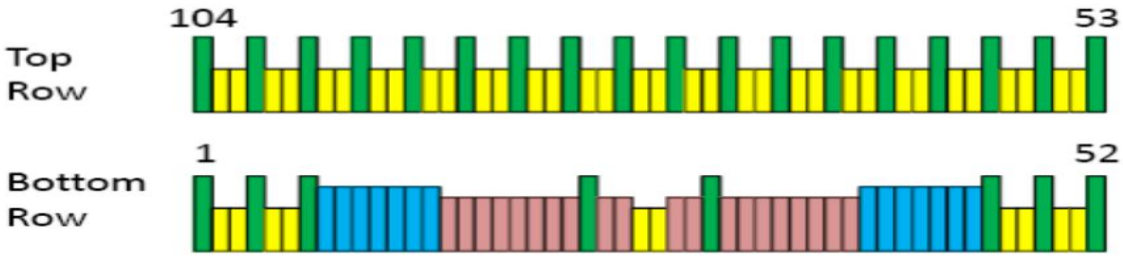

Figure 6. CFP2 Pin Map Connector

	Bottom Row		Bottom Row		Top Row		Top Row
1	GND	52	3.3V_GND	53	GND	104	GND
2	(TX_MCLKn)	51	(RX_MCLKp)	54	N.C.	103	N.C.
3	(TX_MCLKp)	50	(RX_MCLKn)	55	N.C.	102	N.C.
4	GND	49	3.3V_GND	56	GND	101	GND
5	N.C.	48	N.C.	57	RX0p	100	TX3n
6	N.C.	47	N.C.	58	RX0n	99	TX3p
7	3.3V_GND	46	3.3V_GND	59	GND	98	GND
8	3.3V_GND	45	3.3V_GND	60	RX1p	97	TX2n
9	3.3V	44	3.3V	61	RX1n	96	TX2p
10	3.3V	43	3.3V	62	GND	95	GND
11	3.3V	42	3.3V	63	N.C.	94	N.C.
12	3.3V	41	3.3V	64	N.C.	93	N.C.
13	3.3V_GND	40	3.3V_GND	65	GND	92	GND
14	3.3V_GND	39	3.3V_GND	66	N.C.	91	N.C.
15	VND_IO_A	38	VND_IO_E	67	N.C.	90	N.C.
16	VND_IO_B	37	VND_IO_D	68	GND	89	GND
17	PRG-CNTL1	36	VND_IO_C	69	RX2p	88	TX1n
18	PRG-CNTL2	35	PRTADR2	70	RX2n	87	TX1p
19	PRG-CNTL3	34	PRTADR1	71	GND	86	GND
20	PRG-ALRM1	33	PRTADR0	72	RX3p	85	TX0n
21	PRG-ALRM2	32	MDIO	73	RX3n	84	TX0p
22	PRG-ALRM3	31	MDC	74	GND	83	GND
23	GND	30	GND	75	N.C.	82	N.C.
24	TX_DIS	29	MOD_ALRMN	76	N.C.	81	N.C.
25	RX_LOS	28	MOD_RSTn	77	GND	80	GND
26	MOD_LOPWR	27	MOD_ADS	78	(REFCLKp)	79	(REFCLKn)

Figure 7. CFP2 Module Pin Map *Note5

Note5: Pin 15, 16,36,37,38, are internally used and NOT allowed to connect any signal and power supply or GND;
Pin 2, 3, 50, 51 are disabled unless MCLK output is enabled via MDIO.

Pin Function Definitions

Pin Num.	Name	Function	I/O	LOGIC
1,4,23,30,49 52,53,56,59,62 65,68,71,74,77 80,83,86,89,92 95,98,101,104	GND			
2	(TX_MCLKn)	Not Support	O	CML
3	(TX_MCLKp)			
5,6,47,48,54 55,63,64,66,67 75,76,81,82,90 91,93,94,102,103	N.C.	No Connect		
7,8,13,14, 39,40,45,46	3.3V_GND	3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground		
9,10,11,12, 41,42,43,44	3.3V	3.3V Module Supply Voltage		
15	VND_IO_A	Module Vendor I/O. Must No Connect at host board	I/O	
16	VND_IO_B	Module Vendor I/O. Must No Connect at host board	I/O	
17	PRG_CNTL1	Programmable Control 1 set over MDIO, MSA Default: TRXIC_RSTn, TX & RX ICs reset, "0": reset, "1" or NC: enabled = not used , 4.75kohm pull up in the module	I	LVCMOS w/ PUR
18	PRG_CNTL2	Programmable Control 2 set over MDIO, MSA Default: Hardware Interlock LSB, "00": ≤8W, "01":≤16W, "10": ≤ 24W, "11" or NC: ≤32W = not used ,4.75kohm pull up in the module	I	LVCMOS w/ PUR
19	PRG_CNTL3	Programmable Control 3 set over MDIO, MSA Default: Hardware Interlock MSB, "00": ≤8W, "01": ≤16W, "10": ≤ 24W, "11" or NC: ≤32W = not used ,4.75kohm pull up in the module	I	LVCMOS w/ PUR
20	PRG_ALRM1	Programmable Alarm 1 set over MDIO, MSA Default: HIPWR_ON, "1": module power up completed, "0": module not high powered up	O	LVCMOS
21	PRG_ALRM2	Programmable Alarm 2 set over MDIO, MSA Default: MOD_READY, "1": Ready, "0": not Ready.	O	LVCMOS
22	PRG_ALRM3	Programmable Alarm 3 set over MDIO, MSA Default: MOD_FAULT, fault detected, "1": Fault, "0": No Fault	O	LVCOMS
24	TX_DIS	Transmitter Disable for all lanes, "1" or NC = transmitter disabled, "0" = transmitter enabled	I	LVCMOS w/ PUR
25	RX_LOS	Receiver Loss of Optical Signal, "1": low optical signal, "0": normal condition	O	LVCOMS
26	MOD_LOPWR	Module Low Power Mode. "1" or NC: module in low power (safe) mode, "0": power-on enabled 4.75kohm pull up in the module	I	LVCMOS w/ PUR
27	MOD_ABS	Module Absent. "1" or NC: module absent, "0": module present, Pull Up Resistor on Host	O	GND
28	MOD_RSTn	Module Reset. "0" resets the module, "1" or NC = module	I	LVCMOS

		enabled, 4.75kohm Pull Down Resistor in Module		w/ PUR
29	GLB_ALRMn	Global Alarm. "0": alarm condition in any MDIO Alarm register, "1": no alarm condition, Open Drain, Pull Up Resistor on Host	O	LVCOMS
31	MDIO	Management Data I/O bi-directional data (electrical specs as per 802.3ae and 802.3ba)	I/O	1.2V COMS
32	MDC	Management Data Clock (electrical specs as per 802.3ae and 802.3ba)	I	1.2V COMS
33	PRTADR0	MDIO Physical Port address bit 0	I	1.2V COMS
34	PRTADR1	MDIO Physical Port address bit 1	I	1.2V COMS
35	PRTADR2	MDIO Physical Port address bit 2	I	1.2V COMS
50	VND_IO_C	Module Vendor I/O. Must No Connect at host board	I/O	
51	VND_IO_D	Module Vendor I/O. Must No Connect at host board	I/O	
53	VND_IO_E	Module Vendor I/O. Must No Connect at host board	I/O	
50	RX_MCLKn	RX Monitor Clock Output (Negative)	O	
51	RX_MCLKp	RX Monitor Clock Output (Positive)	O	
57	RX0p	Lane 0 Receiver Output (Positive)	O	HS I/O
58	RX0n	Lane 0 Receiver Output (Negative)	O	HS I/O
60	RX1p	Lane 1 Receiver Output (Positive)	O	HS I/O
61	RX1n	Lane 1 Receiver Output (Negative)	O	HS I/O
69	RX2p	Lane 2 Receiver Output (Positive)	O	HS I/O
70	RX2n	Lane 2 Receiver Output (Negative)	O	HS I/O
72	RX3p	Lane 3 Receiver Output (Positive)	O	HS I/O
73	RX3n	Lane 3 Receiver Output (Negative)	O	HS I/O
84	TX0p	Lane 0 Transmitter Input (Positive)	I	HS I/O
85	TX0n	Lane 0 Transmitter Input (Negative)	I	HS I/O
87	TX1p	Lane 1 Transmitter Input (Positive)	I	HS I/O
88	TX1n	Lane 1 Transmitter Input (Negative)	I	HS I/O
96	TX2p	Lane 2 Transmitter Input (Positive)	I	HS I/O
97	TX2n	Lane 2 Transmitter Input (Negative)	I	HS I/O
99	TX3p	Lane 3 Transmitter Input (Positive)	I	HS I/O
100	TX3n	Lane 3 Transmitter Input (Negative)	I	HS I/O
78	REFCLKp	Reference Clock Input (Positive)	I	
79	REFCLKn	Reference Clock Input (Negative)	I	

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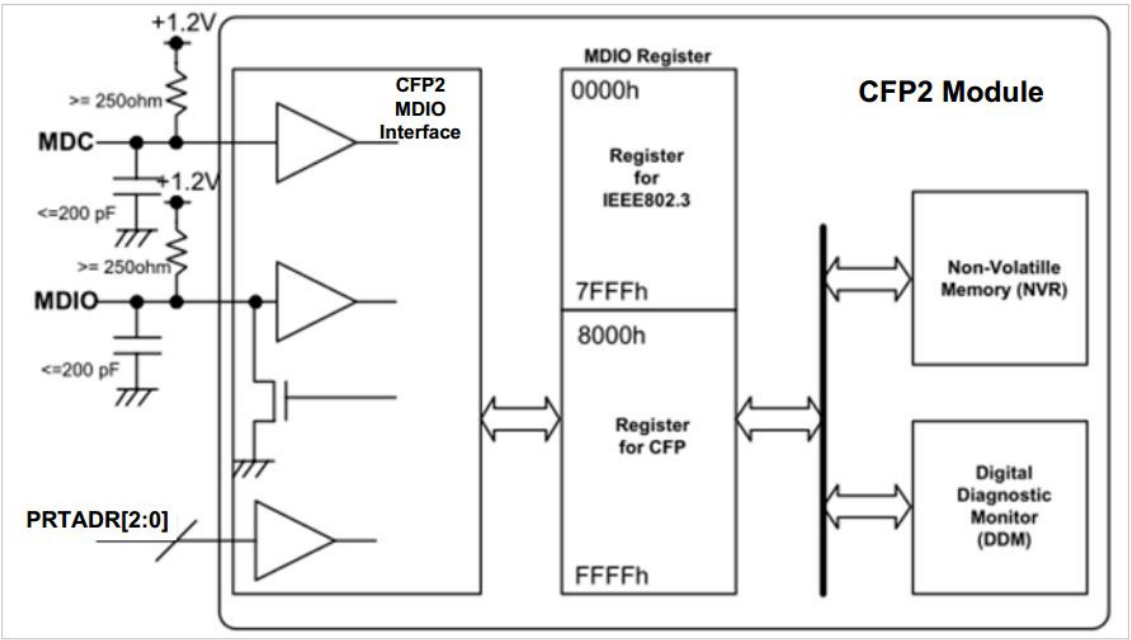
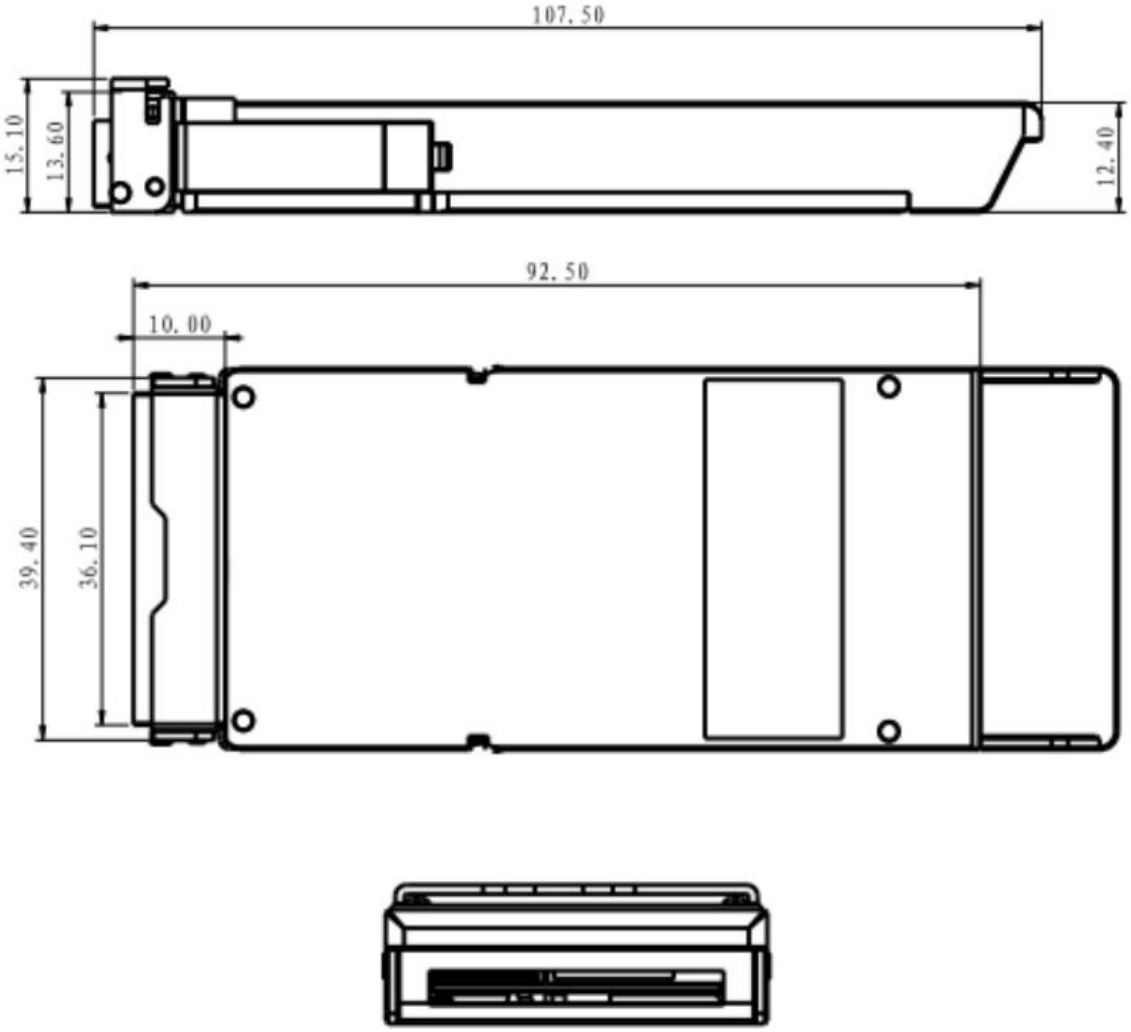
Management Interface

TC2-HG10-31DCR CFP2 transceivers supports the MDIO interface specified in IEEE802.3 Clause 45. This 2-wire management data I/O interface is provided for the module status monitoring and control. The management data clock (MDC) provides clocking for the data that is passed on the MDIO port. Three further pins allow for loading of a port address (PORT_ADDR0-2) into the module.



Mechanical Specifications



Eye Safety

This single-mode transceiver is a Class 1 laser product. It complies with IEC-60825 and FDA 21 CFR 1040.10 and 1040.11. The transceiver must be operated within the specified temperature and voltage limits. The optical ports of the module shall be terminated with an optical connector or with a dust plug.

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